

through-silicon vias, a little primer

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Through-silicon vias (TSV) technology could be present in chips by the end of this year or at least at the beginning of 2008. At least this is what Jan Vardaman, the president and founder of semiconductor packaging consulting firm TechSearch International, concludes in his article titled "3-D Through-Silicon Vias Become a Reality". It is no secret that most designers could envision many ways in which these vertical interconnects could be utilized to decrease timing problems. For example, consider the ever increasing cache sizes that can be found on chips these days. If one could fold these structures in 3D rather than laying them out in 2D, the vertical interconnects could shorten the lengths of global interconnects. Additionally, floor plans could be optimized to arrange units that sit in critical paths to be stacked vertically to reduce routing distance and obtain better timing closure. But so far, while many research projects have been touting the benefits of vertical interconnects, very little of this technology has made it into commercial applications. According to Jan this is likely to change in the near future as TSV technology is moved from the research stage into the commercialization stage.

His article, which is posted over at Semiconductor International, is a short overview of TSV technology, and can be used as a springboard for additional research for the interested reader. Jan gives an extensive summary of companies and institutions that have on-going research on TSV technology. He also gives a nice overview of the three main approaches to TSV, namely a front-end process which uses deep-trench capacitor technology to create the vias, a process where vias are etched through set-aside exclusion zones, and finally a process where vias are created through the redistribution of pads and via streets. It is a relatively short read with some good illustrations so if you are interested in this topic give it a read.